



PATENT
Attorney Docket No. ASC-022CPC1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT(S): Wu *et al.*
SERIAL NO.: 10/603,852 GROUP NO.: 2811
FILING DATE: June 25, 2003 EXAMINER: Not yet assigned
TITLE: ETCH STOP LAYER SYSTEM

CERTIFICATE OF FIRST CLASS MAILING UNDER 37 C.F.R. 1.8

I hereby certify that this correspondence, and any document(s) referred to as enclosed herein, is/are being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 16th day of December, 2003.


Emily K. Walsh

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith are:

1. Transmittal Form (1 pg.);
2. Information Disclosure Statement (2 pgs.);
3. Form PTO-1449 (7 pgs.);
4. Cited References A1-A69, B1-B8, C1-C42;
5. A Return Receipt Postcard; and
6. Certificate of First Class Mailing.



TRANSMITTAL FORM

Application Serial Number	10/603,852
Filing Date	June 25, 2003
First Named Inventor	Wu
Group Art Unit	2811
Examiner Name	Not yet assigned
Attorney Docket No.	ASC-022CPC1
Patent No.	Not applicable
Issue Date	Not applicable

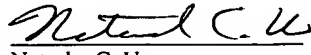
ENCLOSURES (check all that apply)

<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Check Attached <input type="checkbox"/> Copy of Fee Transmittal Form	<input type="checkbox"/> Copy of Notice to File Missing Parts of Application <input type="checkbox"/> Formal Drawing(s) <input type="checkbox"/> Request For Continued Examination (RCE) Transmittal <input type="checkbox"/> Power of Attorney (Revocation of Prior Powers) <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Executed Declaration and Power of Attorney for Utility or Design Patent Application <input type="checkbox"/> Small Entity Statement <input type="checkbox"/> CD(s) for large table or computer program <input type="checkbox"/> Amendment After Allowance <input type="checkbox"/> Request for Certificate of Correction <input type="checkbox"/> Certificate of Correction (in duplicate)	<input type="checkbox"/> Notice of Appeal to Board of Patent Appeals and Interferences <input type="checkbox"/> Appeal Brief (in triplicate) <input type="checkbox"/> Status Inquiry <input checked="" type="checkbox"/> Return Receipt Postcard <input checked="" type="checkbox"/> Certificate of First Class Mailing under 37 C.F.R. 1.8 <input type="checkbox"/> Certificate of Facsimile Transmission under 37 C.F.R. 1.8 <input type="checkbox"/> Additional Enclosure(s) (please identify below)
<input type="checkbox"/> Amendment/Response <input type="checkbox"/> Preliminary <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Letter to Official Draftsperson including Drawings [Total Sheets ____] <input type="checkbox"/> Petition for Extension of Time <input checked="" type="checkbox"/> Information Disclosure Statement <input checked="" type="checkbox"/> Form PTO-1449 <input checked="" type="checkbox"/> Copies of IDS Citations (A1-A69, B1-B8, and C1-C42) <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Sequence Listing submission <input type="checkbox"/> Paper Copy/CD <input type="checkbox"/> Computer Readable Copy <input type="checkbox"/> Statement verifying identity of above		

CORRESPONDENCE ADDRESS

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Respectfully submitted,

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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with the provisions of 37 C.F.R. 1.97 and 1.98, Applicants hereby make of record the patents and publications listed on the accompanying Form PTO-1449, and other information contained herein, for consideration by the Examiner in connection with the examination of the above-identified patent application. Copies of the patents and publications are enclosed.

REMARKS

In accordance with the provisions of 37 C.F.R. 1.97, this statement is being filed (CHECK ONE):

- ☒ (1) within three (3) months of the **filing date** of a national application other than a continued prosecution application under 37 C.F.R. 1.53(d), or within three (3) months of the **date of entry of the national stage** as set forth in 37 C.F.R. 1.491 in an international application, or before the mailing of the **first Office action** on the merits, or before the mailing of a **first Office action** after the filing of a request for continued examination under 37 C.F.R. 1.114; or
- ☐ (2) after the period defined in (1) but before the mailing date of a **final action** or a **notice of allowance** under 37 C.F.R. 1.311, and
- ☐ the requisite Statement is below, **OR**
- ☐ the requisite fee under 37 C.F.R. 1.17(p), namely **\$180.00**, is included herein, or

- ☐ (3) after the mailing date of a **final action** or **notice of allowance** but before the payment of the **issue fee**, **AND**
- ☐ the requisite Statement is below, **AND**
- ☐ the requisite petition fee under 37 C.F.R. 1.17(p), namely **\$180.00** is included herein.

It is respectfully requested that each of the patents and publications listed on the attached Form PTO-1449, and other information contained herein, be made of record in this application.

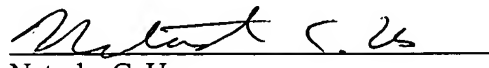
In addition, Applicants wish to inform the Examiner about the following co-pending patent applications, including the office actions issued therein:

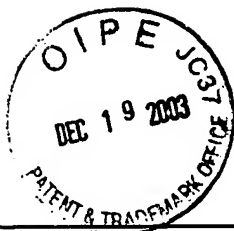
- 1) U.S. Serial No. 09/764,177, filed on 01/07/2001, by Fitzgerald;
- 2) U.S. Serial No. 09/764,182, filed on 01/17/2001, by Fitzgerald (issued as 6,602,613);
- 3) U.S. Serial No. 09/906,545, filed on 07/16/2001, by Fitzgerald;
- 4) U.S. Serial No. 09/906,551, filed on 07/16/2001, by Fitzgerald;
- 5) U.S. Serial No. 09/923,207, filed on 08/06/2001, by Fitzgerald et al. (issued as 6,583,015);
- 6) U.S. Serial No. 09/928,126, filed on 08/10/2001, by Cheng et al. (issued as 6,573,126);
- 7) U.S. Serial No. 10/116,559, filed on 04/04/2002, by Cheng et al.;
- 8) U.S. Serial No. 10/172,542, filed on 06/14/2002, by Hammond et al.;
- 9) U.S. Serial No. 10/264,935, filed on 10/04/2002, by Lochtefeld et al.;
- 10) U.S. Serial No. 09/599,260, filed on 06/22/2000, by Wu et al.; and
- 11) U.S. Serial No. 09/289,514, filed on 04/09/1999, by Wu et al. (issued as 6,521,041).

Respectfully submitted,

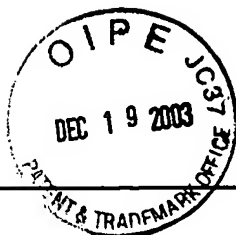
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FORM PTO - 1449				ATTORNEY DOCKET NO.: ASC-022CPC1			
INFORMATION DISCLOSURE STATEMENT				APPLICANT(S): Wu et al.			
				SERIAL NO.: 10/603,852			
				FILING DATE: June 25, 2003		GROUP: 2811	
U.S. PATENT DOCUMENTS							
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A1	4,010,045	03/01/1977	Ruehrwein			
	A2	5,013,681	05/07/1991	Godbey et al.			
	A3	5,166,084	11/24/1992	Pfiester			
	A4	5,202,284	04/13/1993	Kamins et al.			
	A5	5,207,864	05/04/1993	Bhat et al.			
	A6	5,208,182	05/04/1993	Narayan et al.			
	A7	5,212,110	05/18/1993	Pfiester et al.			
	A8	5,221,413	06/22/1993	Brasen et al.			
	A9	5,285,086	02/08/1994	Fitzgerald			
	A10	5,310,451	05/10/1994	Tejwani et al.			
	A11	5,346,848	09/13/1994	Gruppen-Shemansky et al.			
	A12	5,374,564	12/20/1994	Bruel			
	A13	5,413,679	05/09/1995	Godbey			
	A14	5,442,205	08/15/1995	Brasen et al.			
	A15	5,461,243	10/24/1995	Ek et al.			
	A16	5,462,883	10/31/1995	Dennard et al.			
	A17	5,476,813	12/19/1995	Naruse			
	A18	5,484,664	01/16/1996	Kitahara et al.			
	A19	5,523,592	06/04/1996	Nakagawa et al.			
	A20	5,534,713	07/09/1996	Ismail et al.			
	A21	5,536,361	07/16/1996	Kondo et al.			
	A22	5,540,785	07/30/1996	Dennard et al.			
	A23	5,683,934	11/04/1997	Candelaria			
	A24	5,728,623	03/17/1998	Mori			
EXAMINER				DATE CONSIDERED			



FORM PTO - 1449

INFORMATION DISCLOSURE STATEMENT

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U.S. PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A25	5,759,898	06/02/1998	Ek et al.			
	A26	5,792,679	08/11/1998	Nakato			
	A27	5,877,070	03/02/1999	Goesele et al.			
	A28	5,891,769	04/06/1999	Liaw et al.			
	A29	5,906,708	05/25/1999	Robinson et al.			
	A30	5,906,951	05/25/1999	Chu et al.			
	A31	5,943,560	08/24/1999	Chang et al.			
	A32	5,966,622	10/12/1999	Levine et al.			
	A33	5,998,807	12/07/1999	Lustig et al.			
	A34	6,033,974	03/07/2000	Henley et al.			
	A35	6,033,995	03/07/2000	Muller			
	A36	6,059,895	05/09/2000	Chu et al.			
	A37	6,074,919	06/13/2000	Gardner et al.			
	A38	6,096,590	08/01/2000	Chan et al.			
	A39	6,103,559	08/15/2000	Gardner et al.			
	A40	6,107,653	08/22/2000	Fitzgerald			
	A41	6,111,267	08/29/2000	Fischer et al.			
	A42	6,117,750	09/12/2000	Bensahel et al.			
	A43	6,153,495	11/28/2000	Kub et al.			
	A44	6,154,475	11/28/2000	Soref et al.			
	A45	6,162,688	12/19/2000	Gardner et al.			
	A46	6,184,111 B1	02/06/2001	Henley et al.			
	A47	6,191,007 B1	02/20/2001	Matsui et al.			
	A48	6,191,432 B1	02/20/2001	Sugiyama et al.			
	A49	6,194,722 B1	02/27/2001	Howe et al.			
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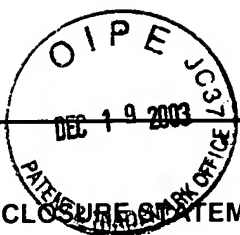
EXAM. INIT.		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	A50	6,207,977	03/27/2001	Augusto			
	A51	6,210,988 B1	04/03/2001	Howe et al.			
	A52	6,218,677 B1	04/17/2001	Broekaert			
	A53	6,232,138 B1	05/15/2001	Fitzgerald et al.			
	A54	6,235,567 B1	05/22/2001	Huang			
	A55	6,251,755 B1	06/26/2001	Furukawa et al.			
	A56	6,261,929 B1	07/17/2001	Gehrke et al.			
	A57	6,291,321 B1	09/18/2001	Fitzgerald			
	A58	6,313,016 B1	11/06/2001	Kibbel et al.			
	A59	6,323,108 B1	11/27/2001	Kub et al.			
	A60	6,335,546 B1	01/01/2002	Tsuda et al.			
	A61	6,350,993 B1	02/26/2002	Chu et al.			
	A62	6,368,733 B1	04/09/2002	Nishinaga			
	A63	6,372,356 B1	04/16/2002	Thornton et al.			
	A65	6,573,126	06/03/2003	Cheng et al.			
	A66	6,583,015	06/24/2003	Fitzgerald et al.			
	A67	2001/0003269 A1	06/14/2001	Wu et al.			
	A68	2002/0125497	09/12/2002	Fitzgerald			
	A69	2003/0013323	01/16/2003	Hammond et al.			

FOREIGN PATENT DOCUMENTS

EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B1	0 587 520	03/16/1994	EP				No	Yes
	B2	0 683 522 A2	11/22/1995	EP				No	Yes

EXAMINER

DATE CONSIDERED



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EXAM. INIT.		DOCUMENT NUMBER	DATE	COUNTRY CODE	CLASS	SUB CLASS	FILING DATE	ABSTRACT ONLY	ENGLISH LANG (Y/N)
	B3	0 828 296	03/11/1998	EP				No	Yes
	B4	2000-31491	01/28/2000	JP				No	Yes
	B5	WO 98/59365	12/30/1998	PCT				No	Yes
	B6	WO 99/53539	10/21/1999	PCT				No	Yes
	B7	WO 00/48239	08/17/2000	PCT				No	Yes
	B8	WO 01/99169	12/27/2001	PCT				No	Yes
OTHER ART, JOURNAL ARTICLES, ETC.									
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)								
	C1	Armstrong, "Technology for SiGe Heterostructure-Based CMOS Devices," Thesis Submitted to the Massachusetts Institute of Technology Department of Electrical Engineering and Computer Science on June 30, 1999, pp. 1-154.							
	C2	Barradas et al., "RBS analysis of MBE-grown SiGe/(001) Si heterostructures with thin, high Ge content SiGe channels for HMOS transistors," <u>Modern Physics Letters B</u> , (2001), abstract.							
	C3	Borenstein et al., "A New Ultra-Hard Etch-Stop Layer for High Precision Micromachining," <u>Proceedings of the 1999 12th IEEE International Conference on Micro Electro Mechanical Systems (MEMS)</u> , January 17-21, 1999, pps. 205-210.							
	C4	Bruel et al., "@SMART CUT: A Promising New SOI Material Technology," <u>Proceedings of the 1995 IEEE International SOI Conference</u> (October 1995), pp. 178-179.							
	C5	Bruel, "Silicon on Insulator Material Technology," <u>Electronic Letters</u> , Vol. 13, No. 14 (July 6, 1995), pp. 1201-1202.							
	C6	Brunner et al., "Molecular beam epitaxy growth and thermal stability of Si _{1-x} Ge _x layers on extremely thin silicon-on-insulator substrates," <u>Thin Solid Films</u> , Vol. 321 (1998), pp. 245-250.							
	C7	Chang et al., "Selective Etching of SiGe/Si Heterostructures," <u>Journal of the Electrochemical Society</u> , No. 1 (January 1991), pp. 202-204.							
	C8	Chen et al., "The Band Model and the Etching Mechanism of Silicon in Aqueous KOH," <u>Journal of the Electrochemical Society</u> , Vol. 142, No. 1 (January 1995), pp. 170-176.							
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OTHER ART, JOURNAL ARTICLES, ETC.			
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)		
	C9	Cheng et al., "Electron Mobility Enhancement in Strained-Si n-MOSFETs Fabricated on SiGe-on-Insulator (SGOI) Substrates," <u>IEEE Electron Device Letters</u> , Vol. 22, No. 7 (July 2001), pp. 321-323.	
	C10	Cheng et al., "Relaxed Silicon-Germanium on Insulator Substrate by Layer Transfer," <u>Journal of Electronic Materials</u> , Vol. 30, No. 12 (2001), pp. L37-L39.	
	C11	Feijoo et al., "Epitaxial Si-Ge Etch Stop Layers with Ethylene Diamine Pyrocatechol for Bonded and Etchback Silicon-on-Insulator," <u>Journal of Electronic Materials</u> , Vol. 23, No. 6 (June 1994), pps. 493-496.	
	C12	Finne et al., "A Water-Amine-Complexing Agent System for Etching Silicon," <u>Journal of the Electrochemical Society</u> , Vol. 114, No. 9 (September 1967), pp. 965-970.	
	C13	Fitzgerald et al., "Relaxed GexSi1-x structures for III-V integration with Si and high mobility two-dimensional electron gases in Si," <u>Journal of Vacuum Science and Technology B</u> , Vol. 10, No. 4 (July/August 1992), pp. 1807-1819.	
	C14	Fitzgerald et al., "Totally Relaxed GexSi1-x Layers with Low Threading Dislocation Densities Grown on Si Substrates," <u>Applied Physics Letters</u> , Vol. 59, No. 7 (August 12, 1991), pps. 811-813.	
	C15	Fukatsu, "SiGe-based semiconductor-on-insulator substrate created by low-energy separation-by-implanted-oxygen," <u>Applied Physics Letters</u> , Vol. 72, No. 26 (June 29, 1998), pp. 3485-3487.	
	C16	Godbey et al., "A Si _{0.7} Ge _{0.3} strained-layer etch stop for the generation of thin layer undoped silicon," <u>Applied Physics Letters</u> , Vol. 56, No. 4 (January 22, 1990), pp. 373-375.	
	C17	Hackbarth et al., "Alternatives to thick MBE-grown relaxed SiGe buffers," <u>Thin Solid Films</u> , Vol. 369, No. 1-2 (July 2000), pp. 148-151.	
	C18	Huang et al., "High-quality strain-relaxed SiGe alloy grown on implanted silicon-on-insulator substrate," <u>Applied Physics Letters</u> , Vol. 76, No. 19 (May 8, 2000), pp. 2680-2682.	
	C19	Ishikawa et al., "Creation of Si-Ge-based SIMOX structures by low energy oxygen implantation," <u>Proceedings of the 1997 IEEE International SOI Conference</u> (October 1997), pp. 16-17.	
	C20	Ishikawa et al., "SiGe-on-insulator substrate using SiGe alloy grown Si(001)," <u>Applied Physics Letters</u> , Vol. 75, No. 7 (August 16, 1999), pp. 983-985.	
	C21	Ismail, "Si/SiGe High-Speed Field-Effect Transistors," Electron Devices Meeting, Washington D.C., December 10, 1995.	
	C22	König et al., "Design Rules for n-Type SiGe Hetero FETs," <u>Solid State Electronics</u> , Vol. 41, No. 10 (1997), pp. 1541-1547.	
	C23	Leancu et al., "Anisotropic etching of germanium," <u>Sensors and Actuators A</u> , Vol. 46-47 (1995), pp. 35-37.	
EXAMINER		DATE CONSIDERED	



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OTHER ART, JOURNAL ARTICLES, ETC.			
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)		
	C24	LeGoues et al., "Relaxation of SiGe thin films grown on Si/SiO ₂ substrates," <u>Applied Physics Letters</u> , Vol. 75, No. 11 (June 1, 1994), pp. 7240-7246.	
	C25	Leitz et al., "Dislocation glide and blocking kinetics in compositionally graded SiGe/Si," <u>Journal of Applied Physics</u> , Vol. 90, No. 6 (September 15, 2001), pp. 2730-2736.	
	C26	Maiti et al., "Strained-Si heterostructure field effect transistors," <u>Semiconductor Science and Technology</u> , Vol. 13 (1998), pp. 1225-1246.	
	C27	Mazara, "Silicon-On-Insulator by Wafer Bonding: A Review," <u>Journal of the Electrochemical Society</u> , No. 1 (January 1991), pp. 341-347.	
	C28	Mizuno et al., "Electron and Hole Mobility Enhancement in Strained-Si MOSFET's on SiGe-on-Insulator Substrates Fabricated by SIMOX Technology," <u>IEEE Electron Device Letters</u> , Vol. 21, No. 5 (May 2000), pp. 230-232.	
	C29	Narozny et al., "Si/SiGe Heterojunction Bipolar Transistor with Graded GAP SiGe Base Made by Molecular Beam Epitaxy," <u>IEEE IEDM</u> (1988), pp. 562-565.	
	C30	Powell et al., "New approach to the growth of low dislocation relaxed SiGe material," <u>Applied Physics Letters</u> , Vol. 64, No. 14 (April 4, 1994), pp. 1865-1858.	
	C31	Rim et al., "Fabrication and Analysis of Deep Submicron Strained-Si N-MOSFET's," <u>IEEE Transactions on Electron Devices</u> , Vol. 47, No. 7 (July 2000), pp. 1406-1415.	
	C32	Sadek et al., "Design of Si/SiGe Heterojunction Complementary Metal-Oxide-Semiconductor Transistors," <u>IEEE Trans. Electron Devices</u> , Vol. 43, No. 8 (August 1996), pp. 1224-1232.	
	C33	Seidel et al., "Anisotropic Etching of Crystalline Silicon in Alkaline Solutions," <u>Journal of the Electrochemical Society</u> , Vol. 137, No. 11 (November 1990), pp. 3626-3632.	
	C34	Shang et al., "The Development of an Anisotropic Si Etch Process Selective to Ge _x Si _{1-x} Underlayers," <u>Journal of the Electrochemical Society</u> , Vol. 141, No. 2 (February 1994), pp. 507-510.	
	C35	Takagi et al., "On the Universality of Inversion Layer Mobility in Si MOSFET's: Part I-Effects of Substrate Impurity Concentration," <u>IEEE Transactions on Electron Devices</u> , Vol. 41, No. 12 (December 1994), pp. 2357-2362.	
	C36	Ting et al., "Monolithic Integration of III-V Materials and Devices on Silicon," Part of the SPIE Conference on Silicon-Based Optoelectronics, San Jose, CA, (January 1999), pp. 19-28.	
	C37	Usami et al., "Spectroscopic study of Si-based quantum wells with neighboring confinement structure," <u>Semiconductor Science and Technology</u> , (1997), abstract.	
	C38	Wu, "Novel Etch-Stop Materials for Silicon Micromachining," Thesis Submitted to the Massachusetts Institute of Technology Department of Materials Science and Engineering on May 9, 1997, pp. 1-62.	
EXAMINER		DATE CONSIDERED	



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OTHER ART, JOURNAL ARTICLES, ETC.			
EXAM. INIT.	OTHER DOCUMENTS: (Including Author, Title, Date, Relevant Pages, Place of Publication)		
	C39	Yeo et al., "Nanoscale Ultra-Thin-Body Silicon-on-Insulator P-MOSFET with a SiGe/Si Heterostructure Channel," <u>IEEE Electron Device Letters</u> , Vol. 21, No. 4 (April 2000), pp. 161-163.	
	C40	Yi et al., "Si _{1-x} Ge _x /Si Multiple Quantum Well Wires Fabricated Using Selective Etching," <u>Materials Research Society Symposium Proceedings</u> , Vol. 379 (1995), pp. 91-96.	
	C41	Zhang et al., "Demonstration of a GaAs-Based Compliant Substrate Using Wafer Bonding and Substrate Removal Techniques," Electronic Materials and Processing Research Laboratory, Department of Electrical Engineering, University Park, PA 16802, (1998), pp. 25-28.	
	C42	IBM Technical Disclosure Bulletin, Vol. 32, No. 8A, January 1990, "Optimal Growth Technique and Structure for Strain Relaxation of Si-Ge Layers on Si Substrates," pp. 330-331.	
EXAMINER		DATE CONSIDERED	

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